FIG. 1

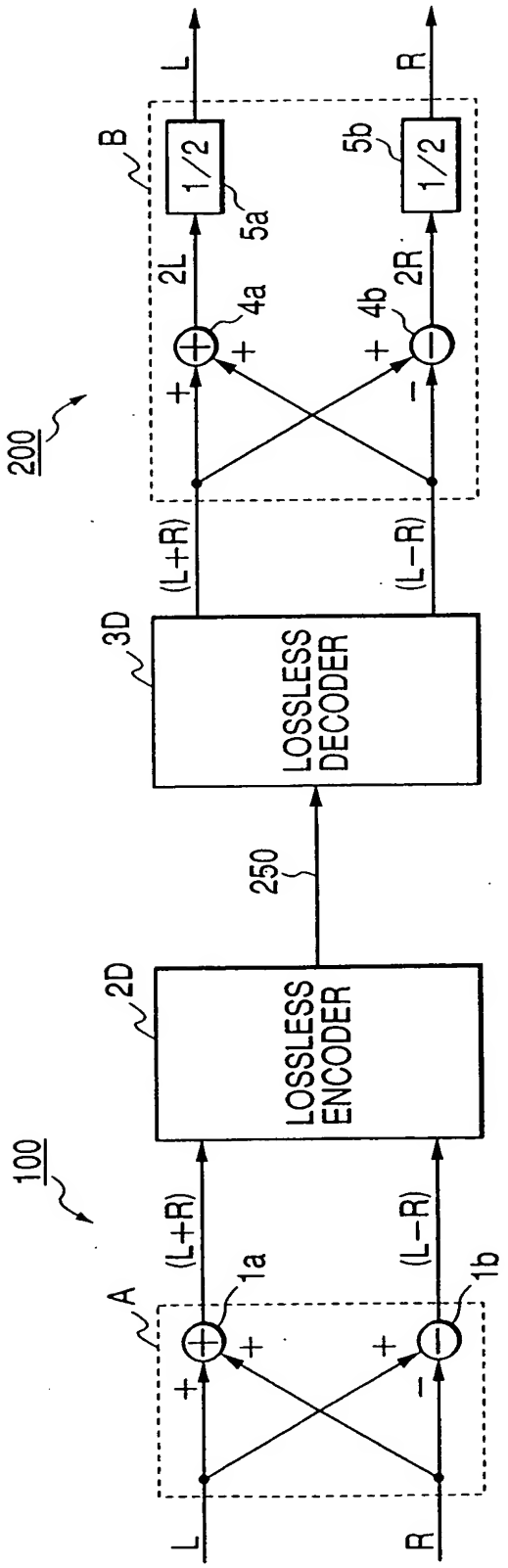

100
200
A
B
1a
1b
4a
4b
5a
5b
2D
3D
250
LOSSLESS ENCODER
LOSSLESS DECODER
(L+R)
(L−R)
2L
2R
1/2
L
R
+
−

FIG. 2

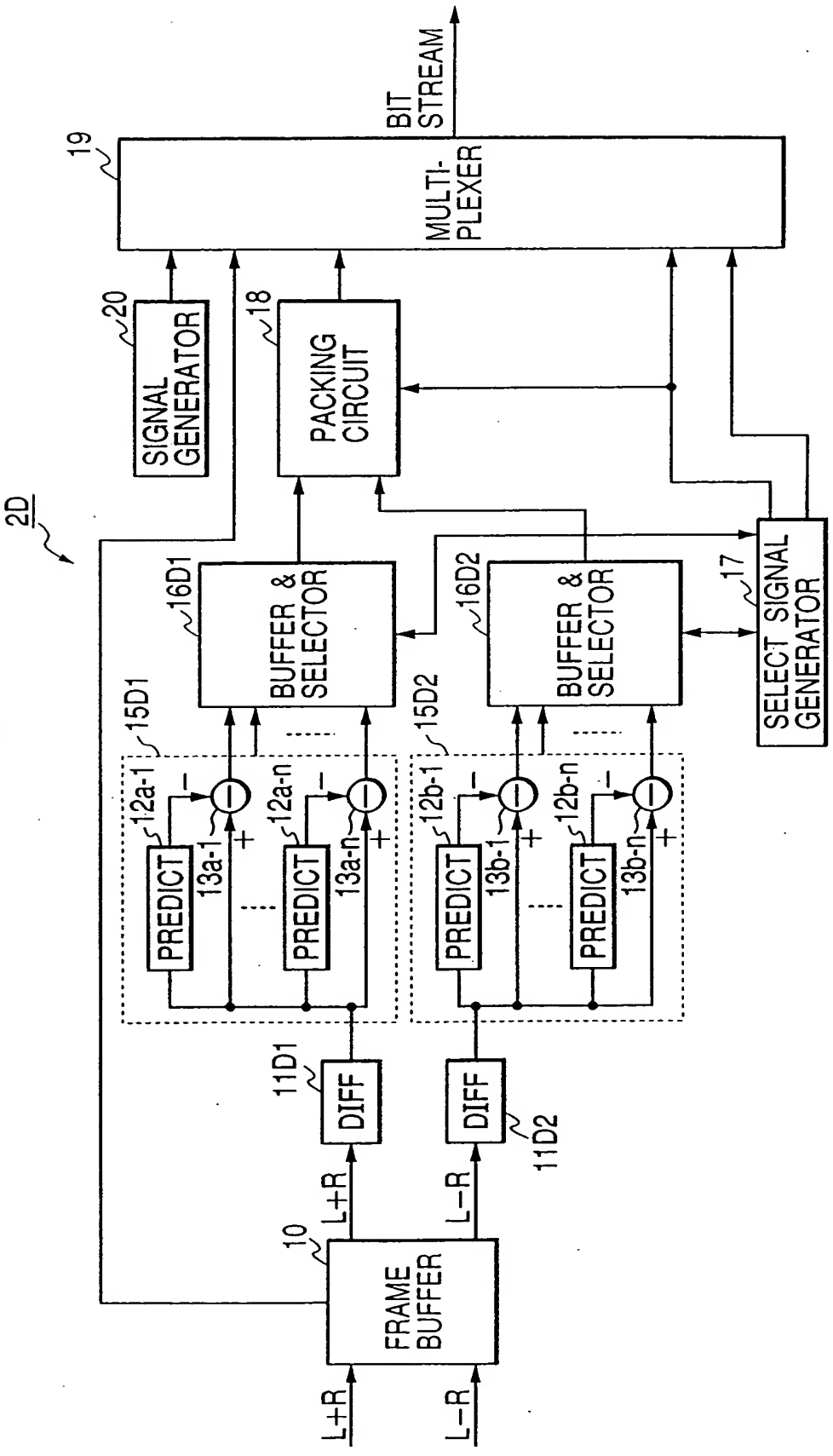

2D
L+R
L−R
10
FRAME BUFFER
11D1
DIFF
11D2
DIFF
15D1
15D2
12a-1
12a-n
12b-1
12b-n
13a-1
13a-n
13b-1
13b-n
PREDICT
16D1
BUFFER & SELECTOR
16D2
BUFFER & SELECTOR
17
SELECT SIGNAL GENERATOR
18
PACKING CIRCUIT
19
MULTI-PLEXER
20
SIGNAL GENERATOR
BIT STREAM

FIG. 3

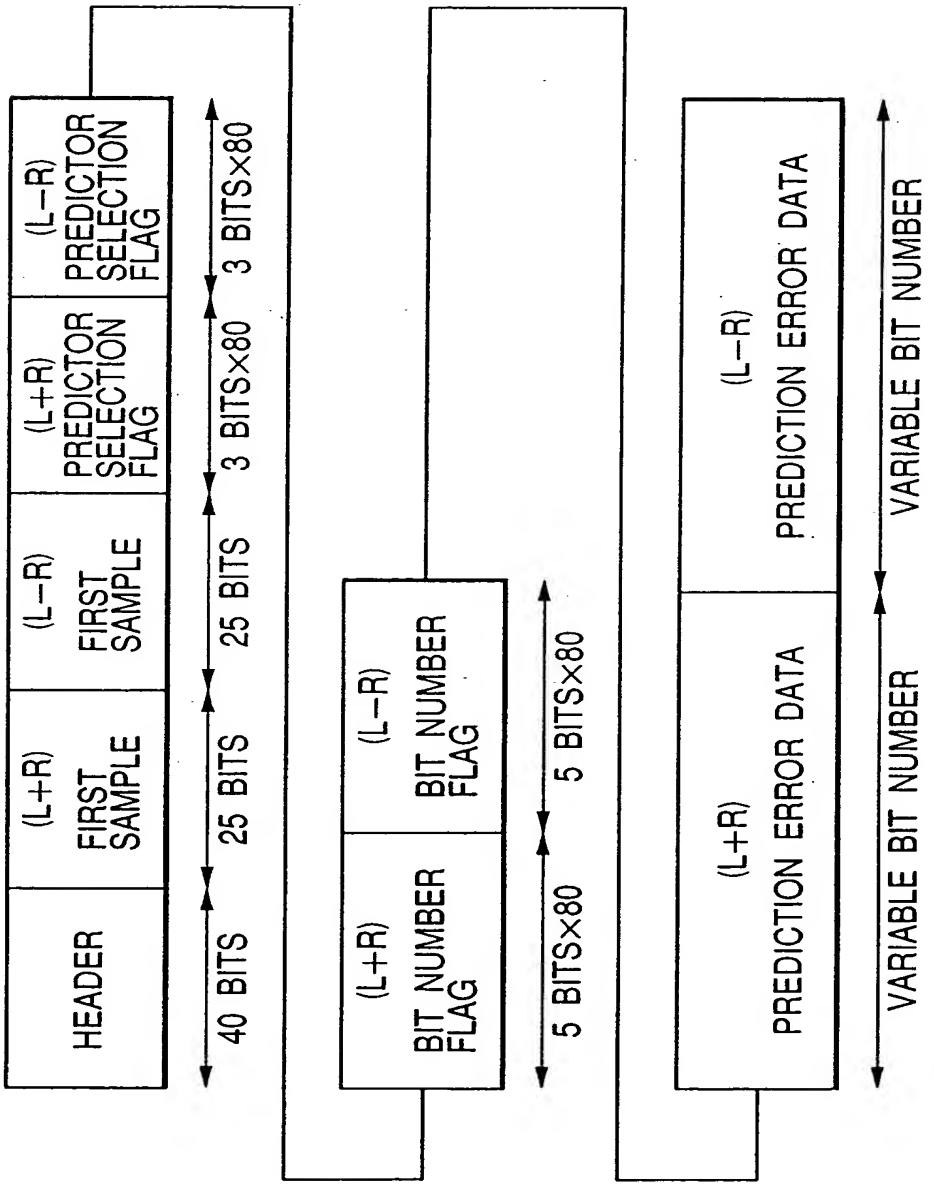

HEADER
(L+R) FIRST SAMPLE
(L−R) FIRST SAMPLE
(L+R) PREDICTOR SELECTION FLAG
(L−R) PREDICTOR SELECTION FLAG
40 BITS
25 BITS
25 BITS
3 BITS×80
3 BITS×80
(L+R) BIT NUMBER FLAG
(L−R) BIT NUMBER FLAG
5 BITS×80
5 BITS×80
(L+R) PREDICTION ERROR DATA
(L−R) PREDICTION ERROR DATA
VARIABLE BIT NUMBER
VARIABLE BIT NUMBER

FIG. 4

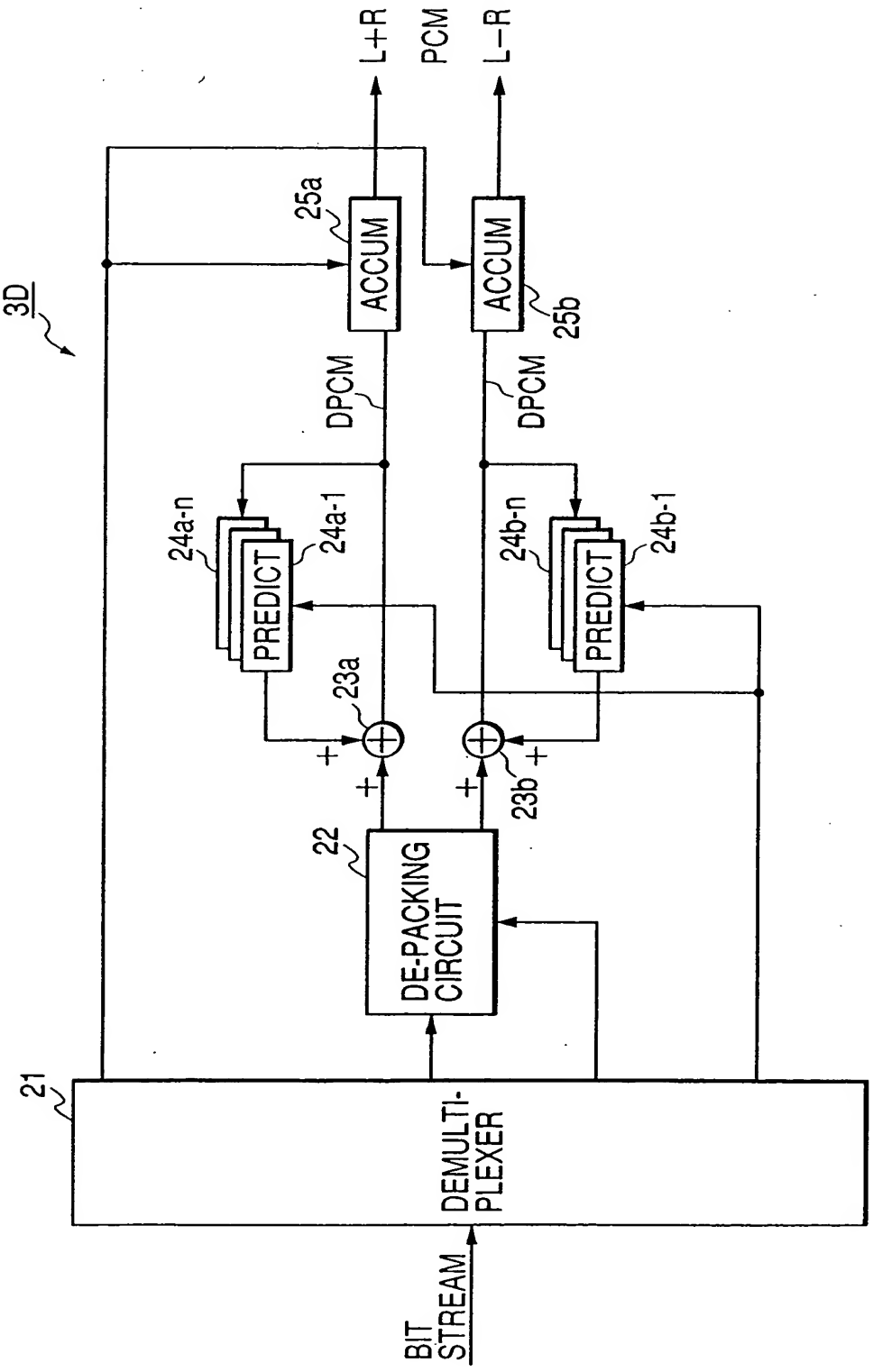

3D
21
DEMULTI-PLEXER
BIT STREAM
22
DE-PACKING CIRCUIT
23a
23b
24a-1
24a-n
24b-1
24b-n
PREDICT
25a
25b
ACCUM
DPCM
DPCM
L+R
PCM
L−R

FIG. 5

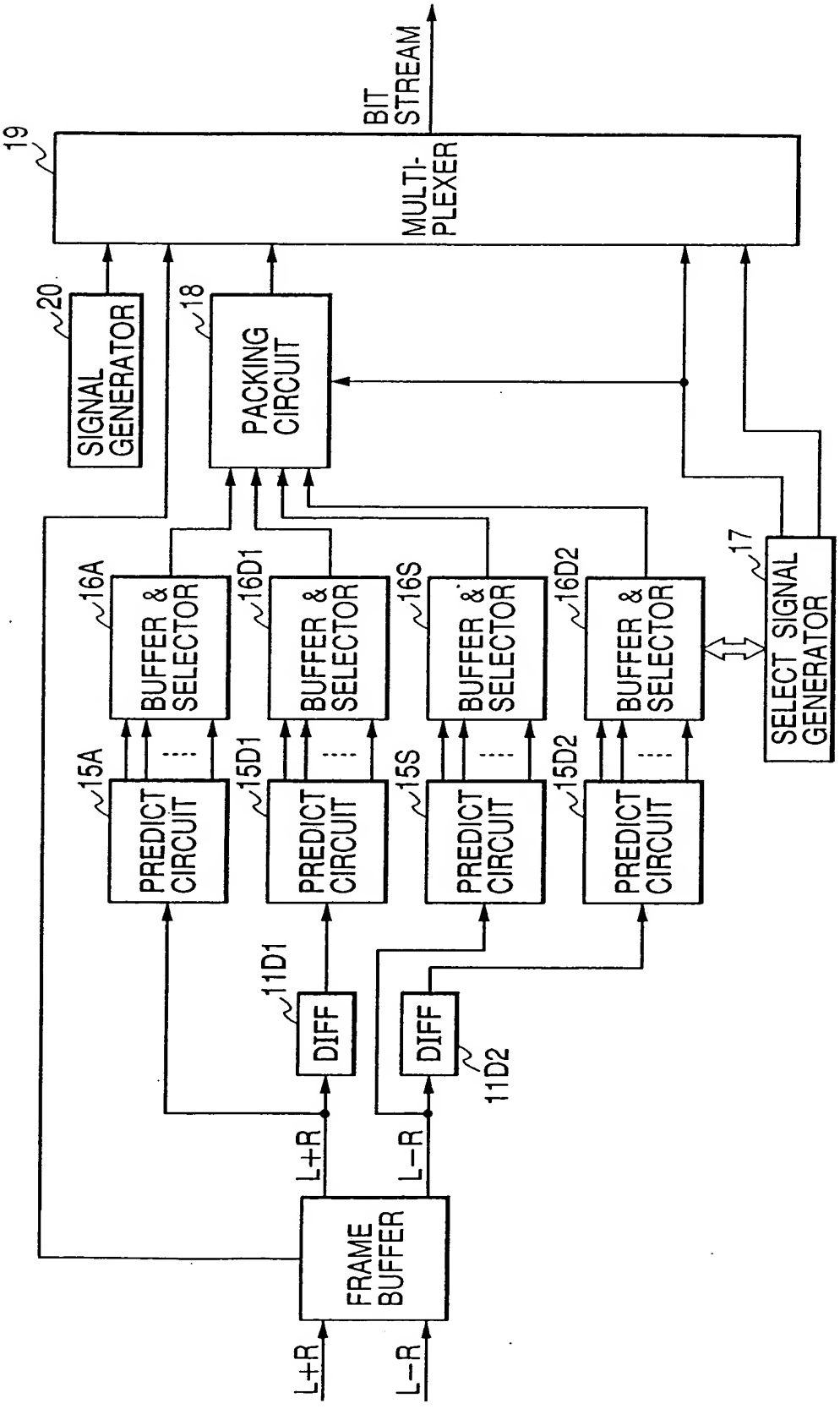

BIT STREAM
19
MULTI-PLEXER
20
SIGNAL GENERATOR
18
PACKING CIRCUIT
16A
BUFFER & SELECTOR
16D1
BUFFER & SELECTOR
16S
BUFFER & SELECTOR
16D2
BUFFER & SELECTOR
17
SELECT SIGNAL GENERATOR
15A
PREDICT CIRCUIT
15D1
PREDICT CIRCUIT
15S
PREDICT CIRCUIT
15D2
PREDICT CIRCUIT
11D1
DIFF
11D2
DIFF
L+R
L−R
FRAME BUFFER
L+R
L−R

FIG. 6

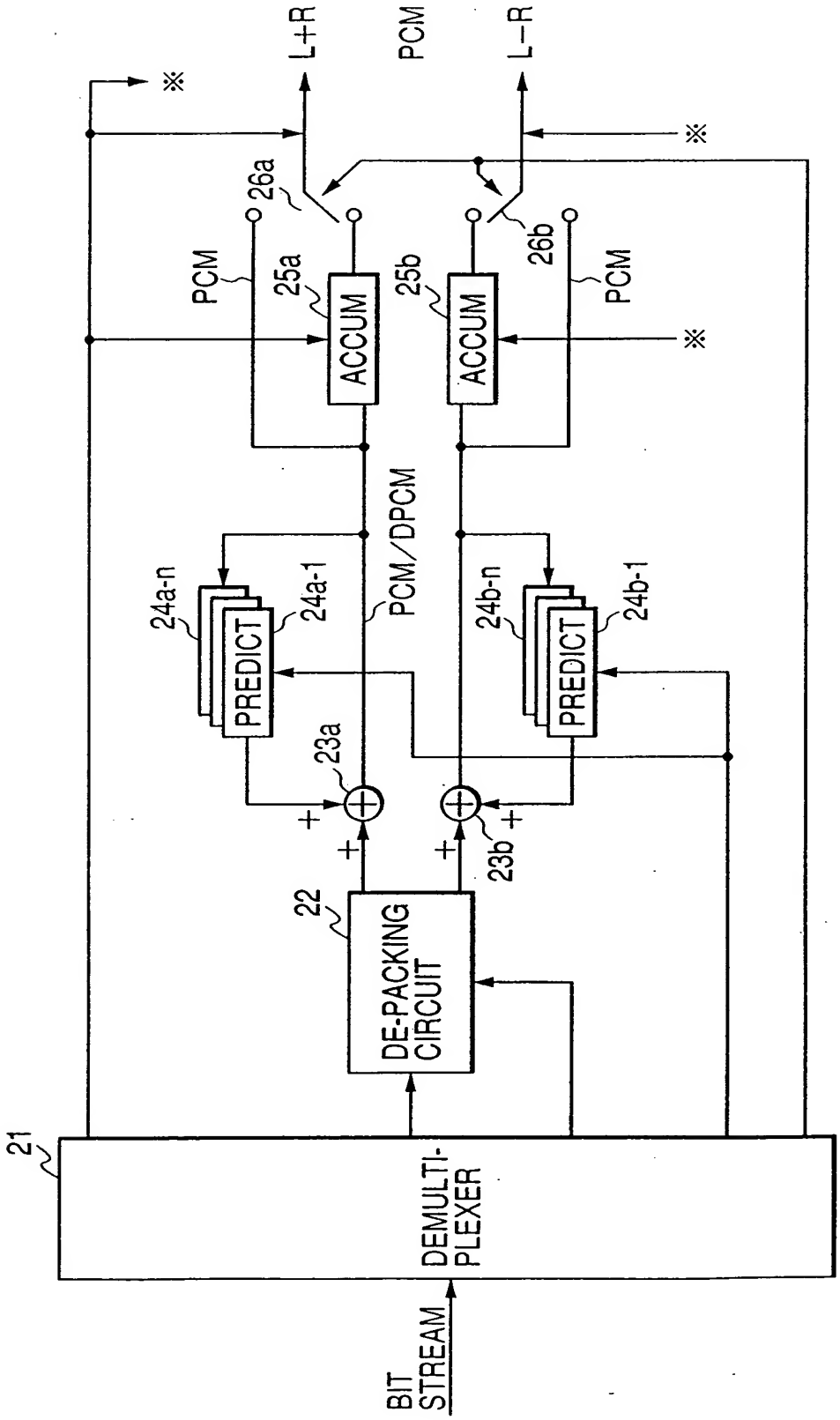

BIT STREAM
21
DEMULTI-PLEXER
22
DE-PACKING CIRCUIT
23a
23b
24a-n
24a-1
PREDICT
24b-n
24b-1
PREDICT
PCM/DPCM
25a
ACCUM
25b
ACCUM
26a
26b
PCM
PCM
L+R
PCM
L−R
※
※
※

FIG. 7

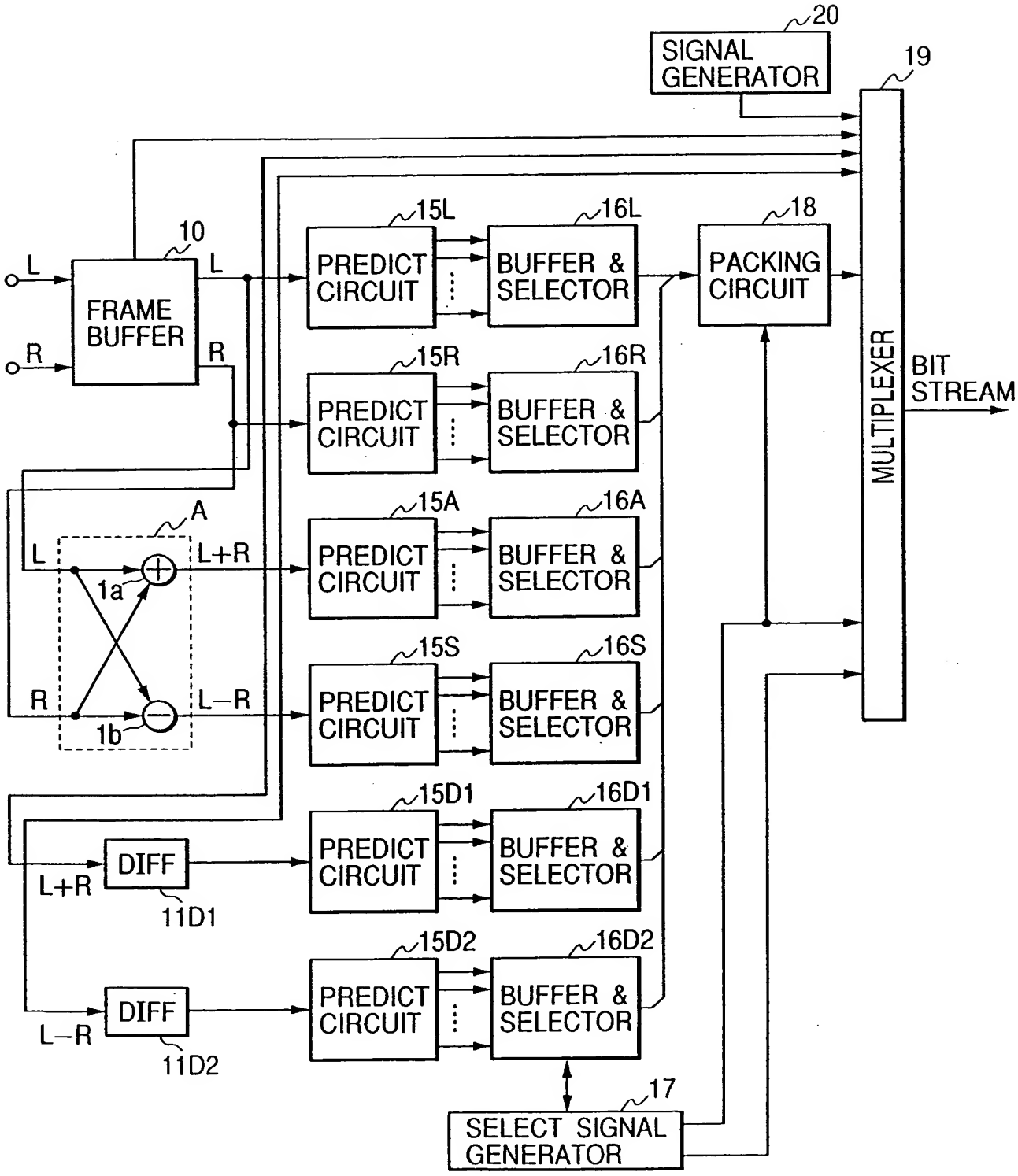

20
SIGNAL GENERATOR
19
MULTIPLEXER
BIT STREAM
10
FRAME BUFFER
L
R
15L
PREDICT CIRCUIT
16L
BUFFER & SELECTOR
18
PACKING CIRCUIT
15R
16R
15A
16A
15S
16S
15D1
16D1
15D2
16D2
A
1a
1b
L+R
L−R
DIFF
11D1
11D2
17
SELECT SIGNAL GENERATOR

FIG. 8

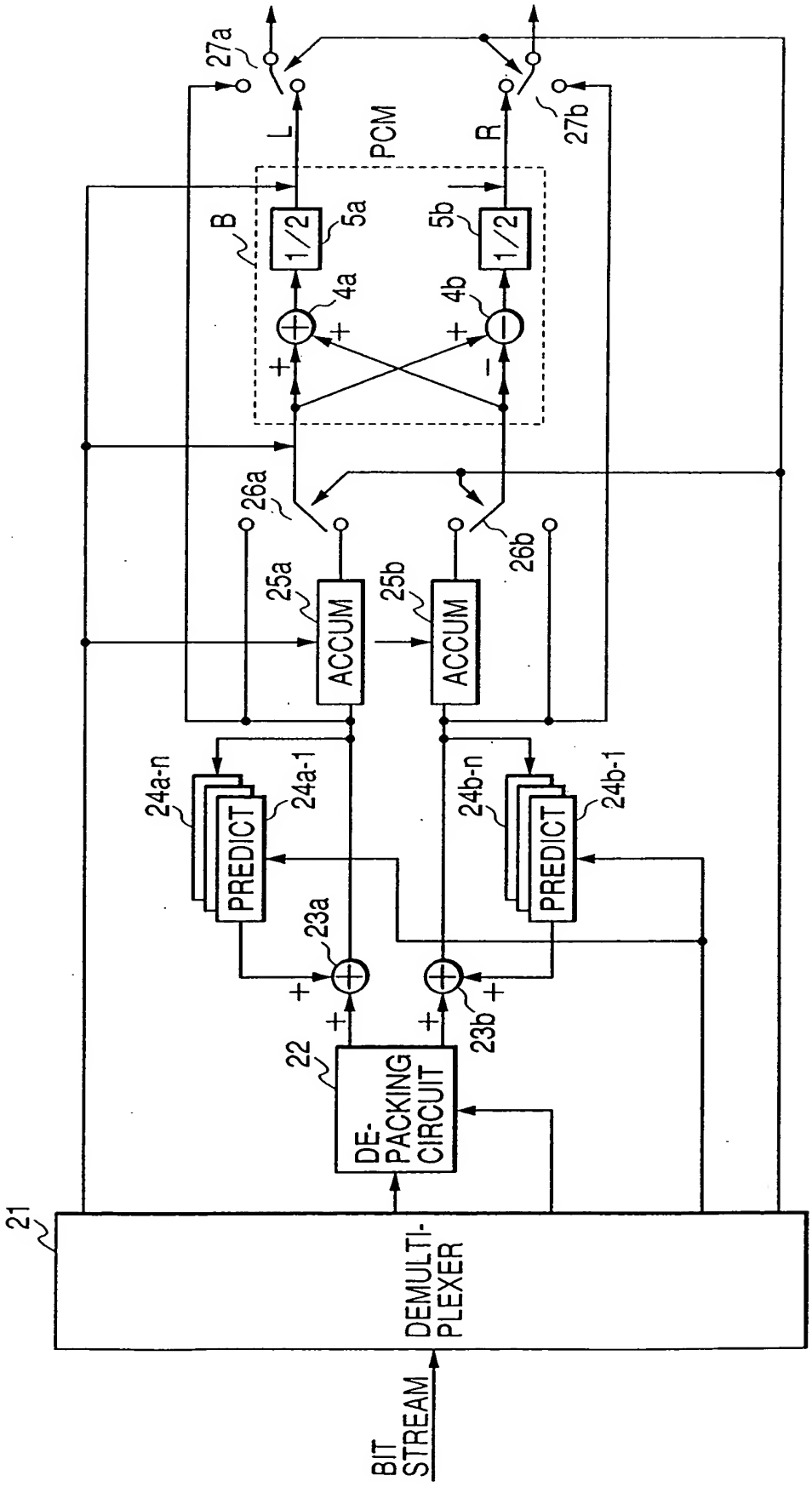

BIT STREAM
21
DEMULTI-PLEXER
22
DE-PACKING CIRCUIT
23a
23b
24a-n
24a-1
24b-n
24b-1
PREDICT
25a
25b
ACCUM
26a
26b
27a
27b
PCM
L
R
B
1/2
5a
5b
4a
4b
+
+
+
+
+
−

FIG. 9

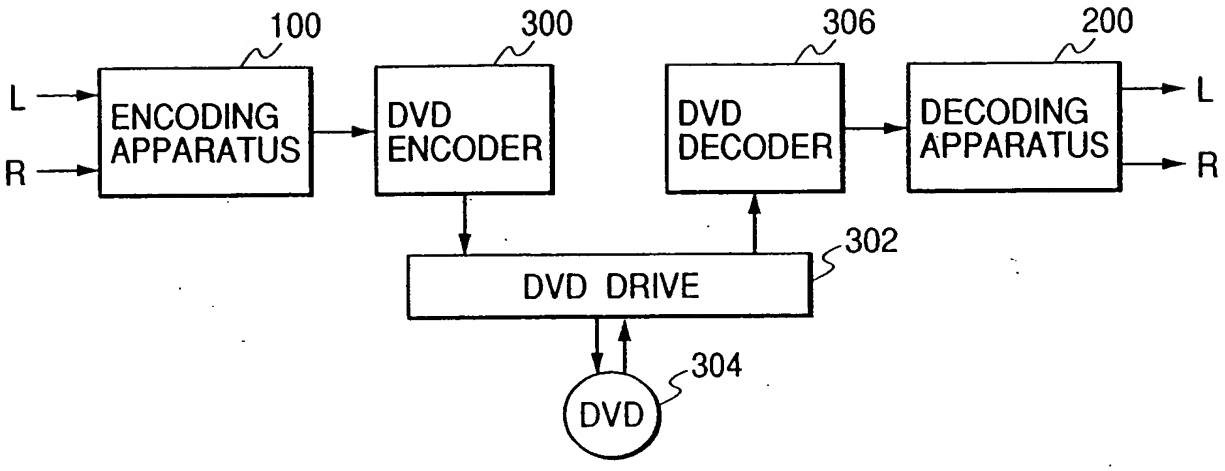


FIG. 10

AUDIO PACK

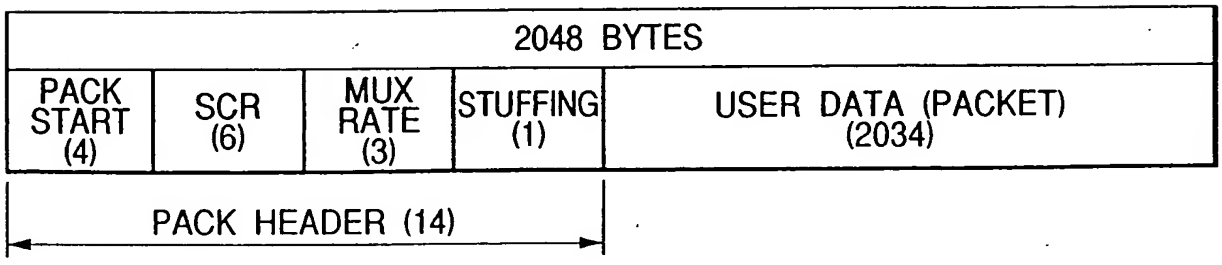


FIG. 11

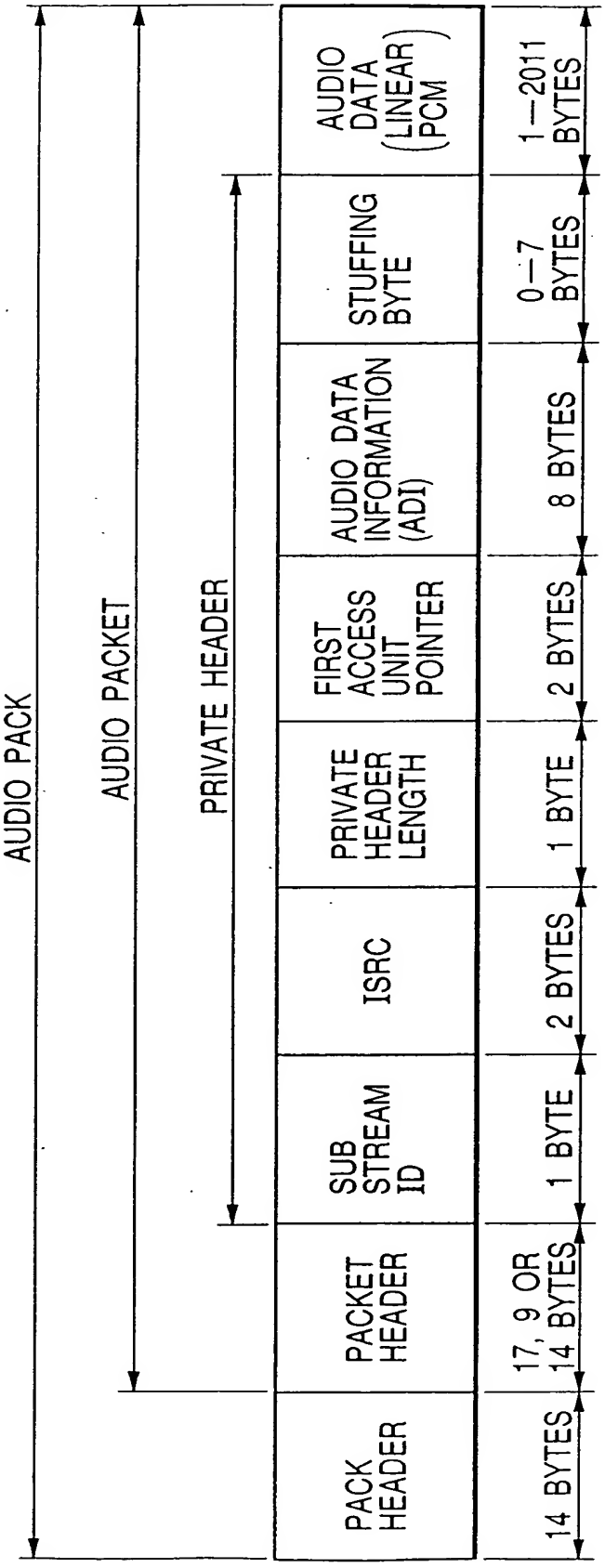

AUDIO PACK
AUDIO PACKET
PRIVATE HEADER
PACK HEADER
PACKET HEADER
SUB STREAM ID
ISRC
PRIVATE HEADER LENGTH
FIRST ACCESS UNIT POINTER
AUDIO DATA INFORMATION (ADI)
STUFFING BYTE
AUDIO DATA (LINEAR PCM)
14 BYTES
17, 9 OR 14 BYTES
1 BYTE
2 BYTES
1 BYTE
2 BYTES
8 BYTES
0—7 BYTES
1—2011 BYTES

FIG. 12

L
R
100
ENCODING APPARATUS
350
PACKETING PROCESSOR
360
NETWORK
370
DE-PACKETING PROCESSOR
200
DECODING PROCESSOR
L
R

FIG. 13

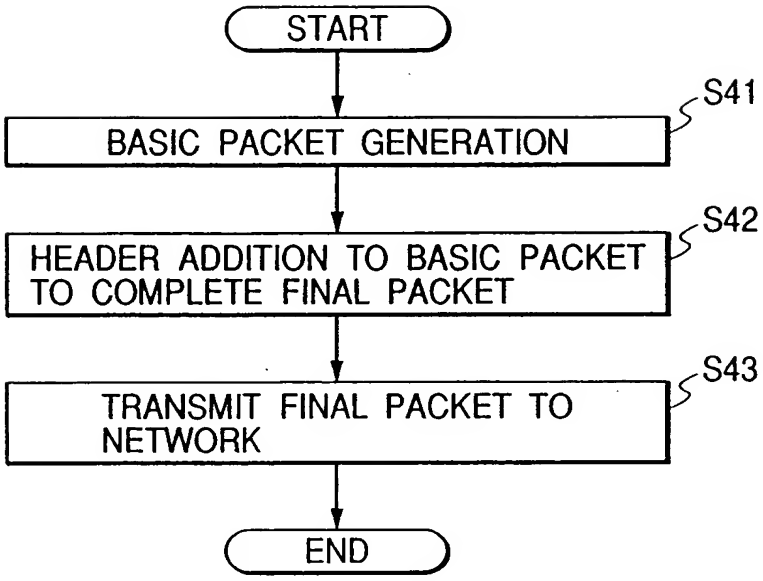

START
S41
BASIC PACKET GENERATION
S42
HEADER ADDITION TO BASIC PACKET TO COMPLETE FINAL PACKET
S43
TRANSMIT FINAL PACKET TO NETWORK
END

FIG. 14

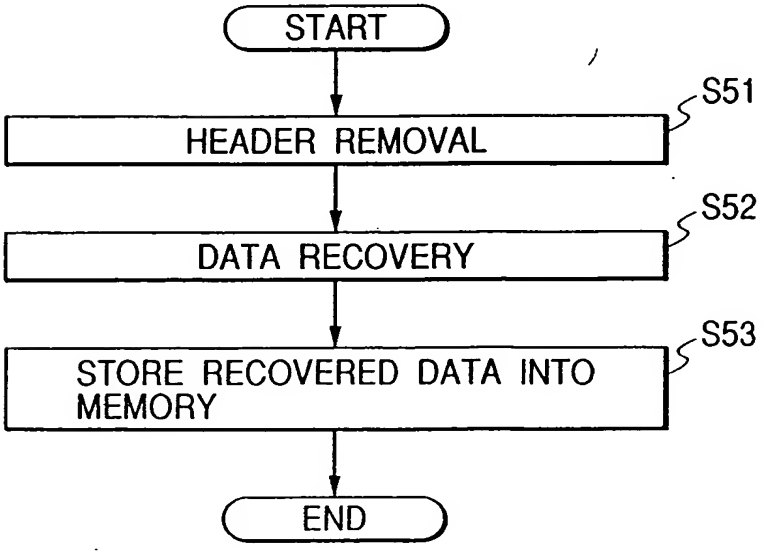

START
S51
HEADER REMOVAL
S52
DATA RECOVERY
S53
STORE RECOVERED DATA INTO MEMORY
END

FIG. 15

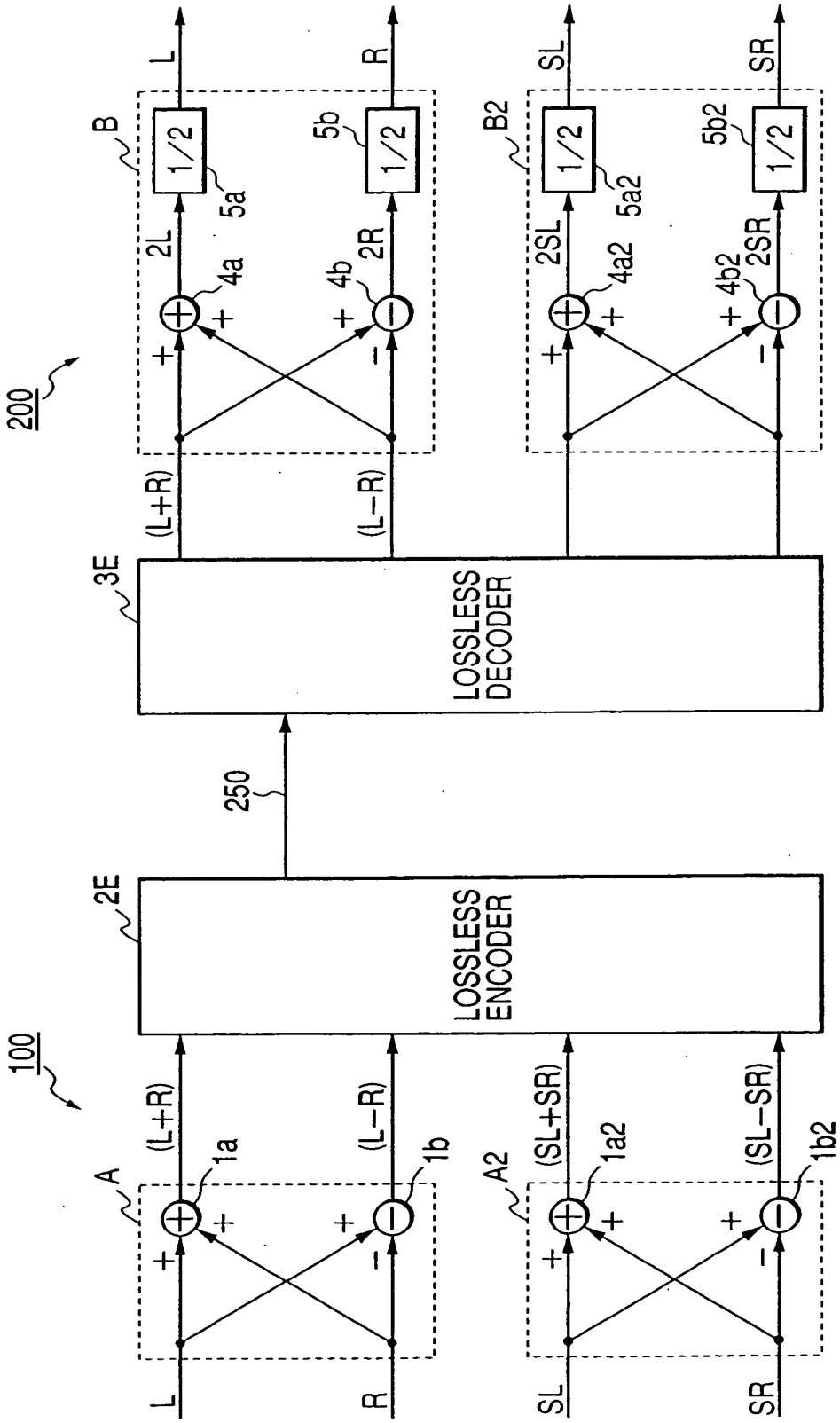

100
200
A
A2
B
B2
1a
1b
1a2
1b2
4a
4b
4a2
4b2
5a
5b
5a2
5b2
1/2
(L+R)
(L−R)
(SL+SR)
(SL−SR)
2L
2R
2SL
2SR
L
R
SL
SR
2E
LOSSLESS ENCODER
250
3E
LOSSLESS DECODER

FIG. 16

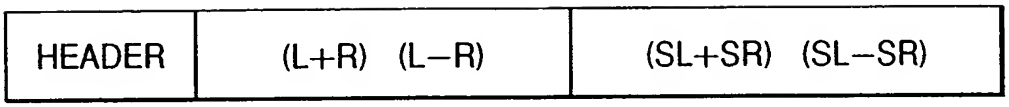


FIG. 18

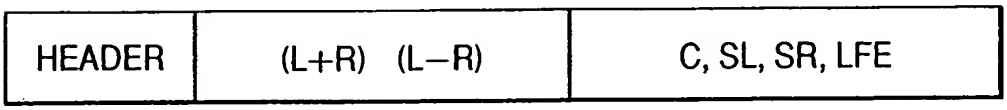


FIG. 17

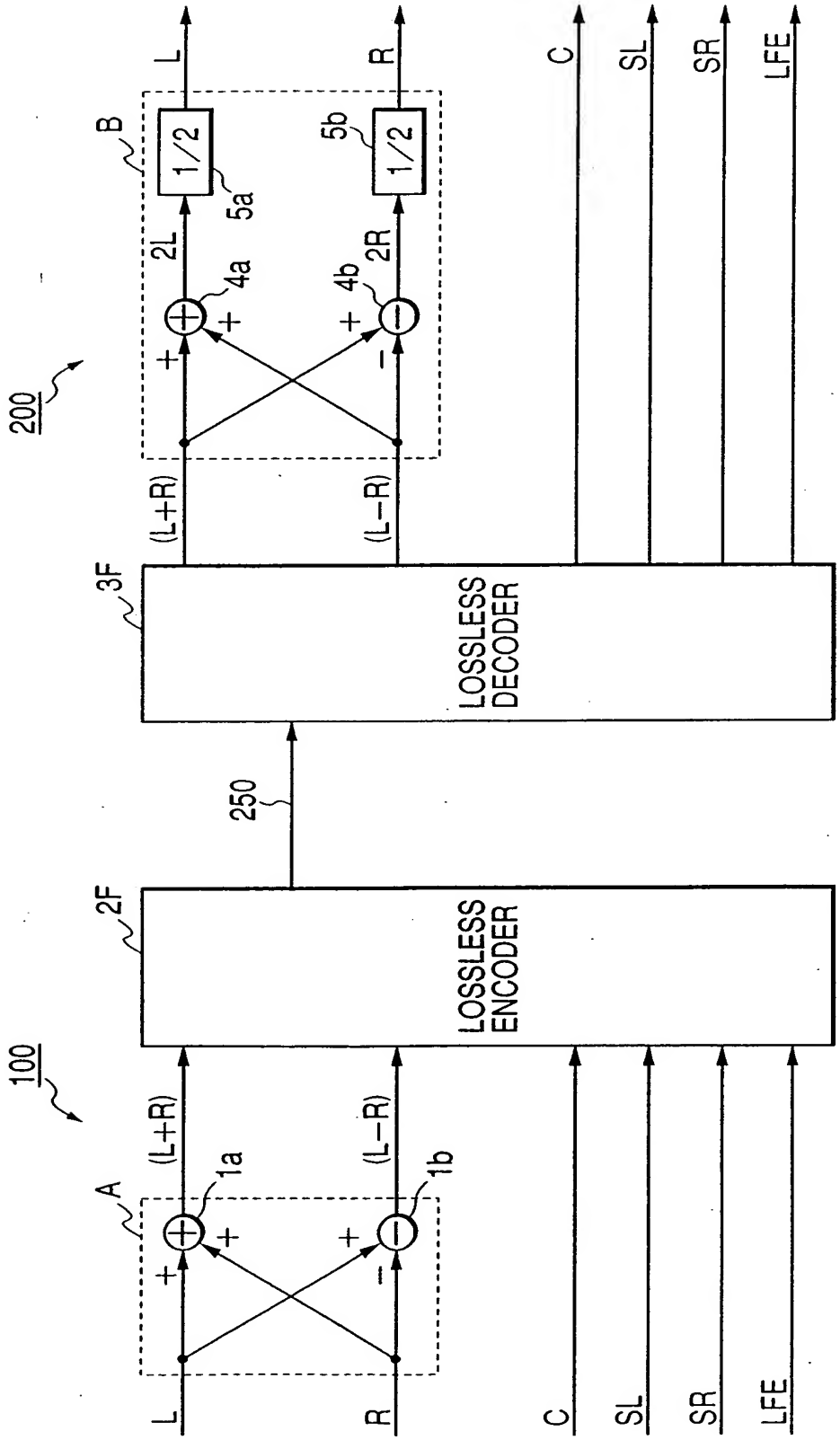

100
200
250
A
B
1a
1b
4a
4b
5a
5b
1/2
1/2
(L+R)
(L−R)
2L
2R
L
R
C
SL
SR
LFE
2F
3F
LOSSLESS ENCODER
LOSSLESS DECODER

FIG. 19

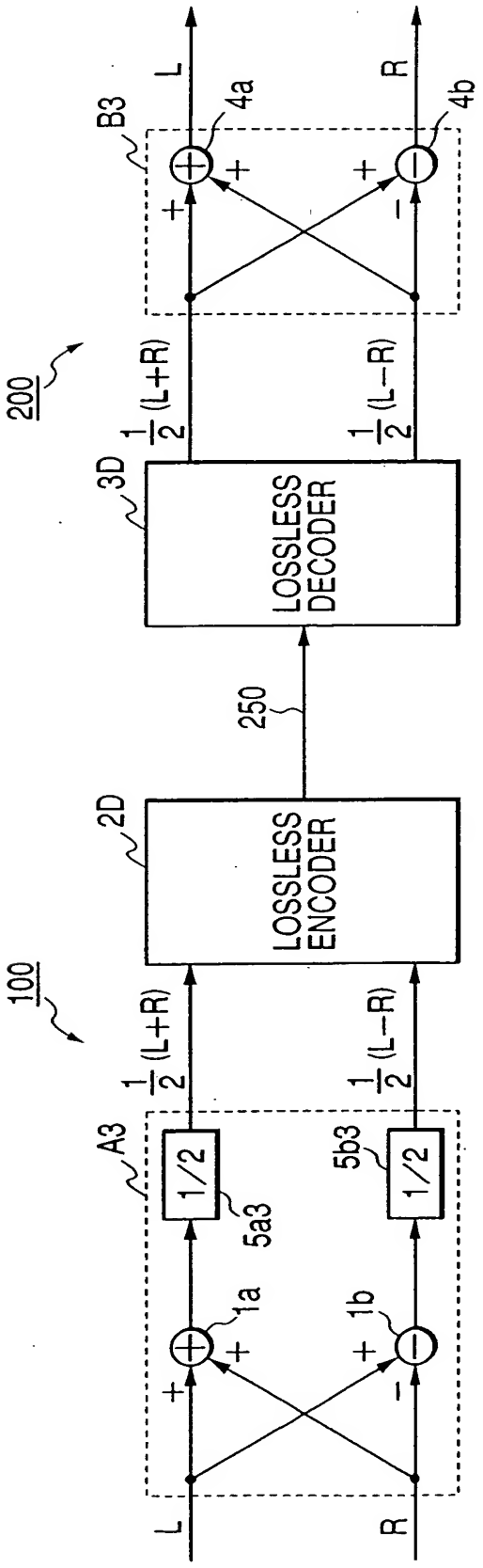
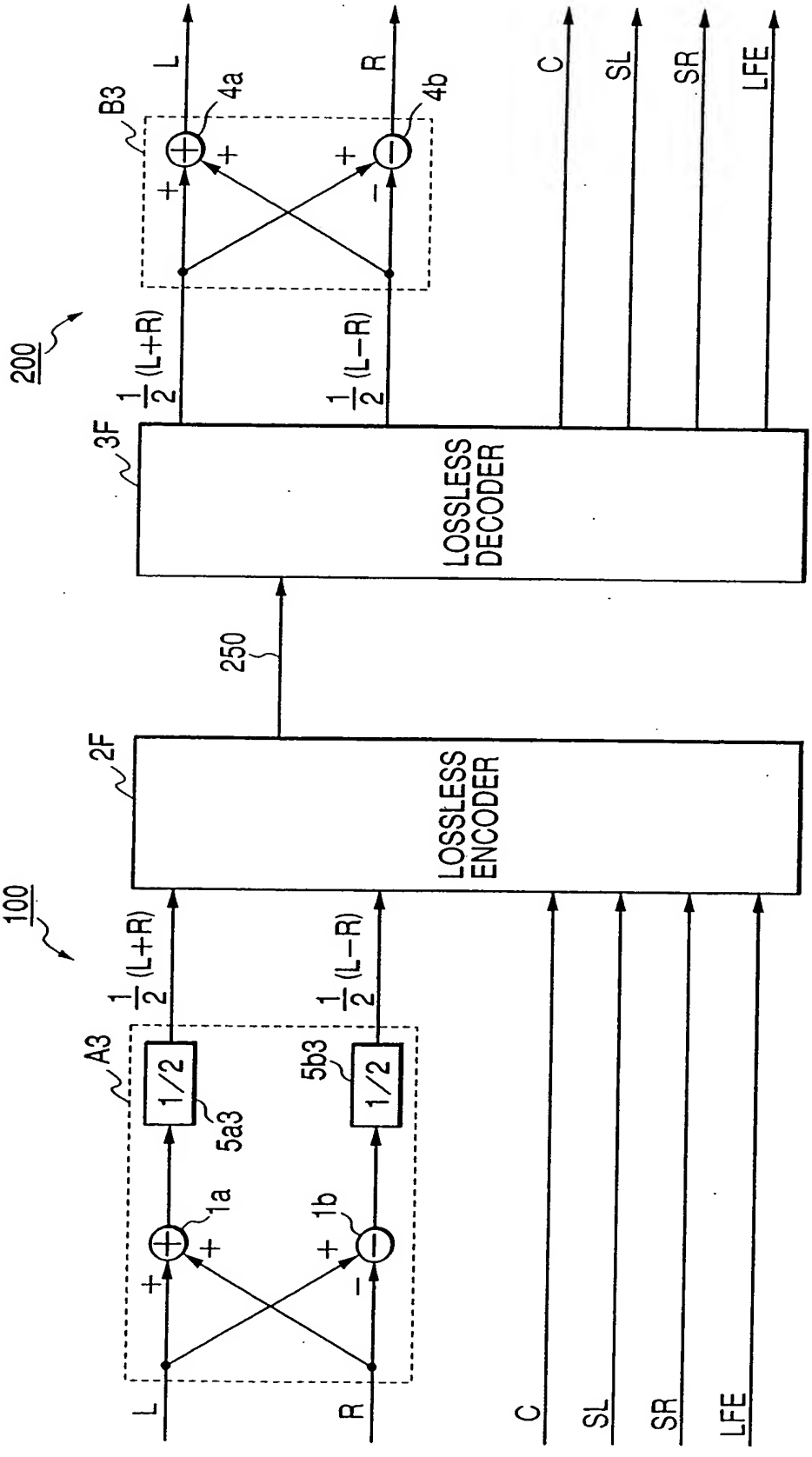

100
200
L
R
A3
1/2
5a3
1a
+
+
5b3
1/2
1b
+
−
1/2 (L+R)
1/2 (L−R)
2D
LOSSLESS ENCODER
250
3D
LOSSLESS DECODER
1/2 (L+R)
1/2 (L−R)
B3
4a
4b
L
R

FIG. 20


100
200
A3
B3
1/2
5a3
5b3
1a
1b
4a
4b
2F
3F
250
LOSSLESS ENCODER
LOSSLESS DECODER
L
R
C
SL
SR
LFE
1/2 (L+R)
1/2 (L−R)